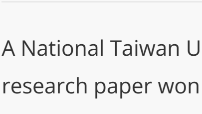
Lack of standardized methods, reportin...

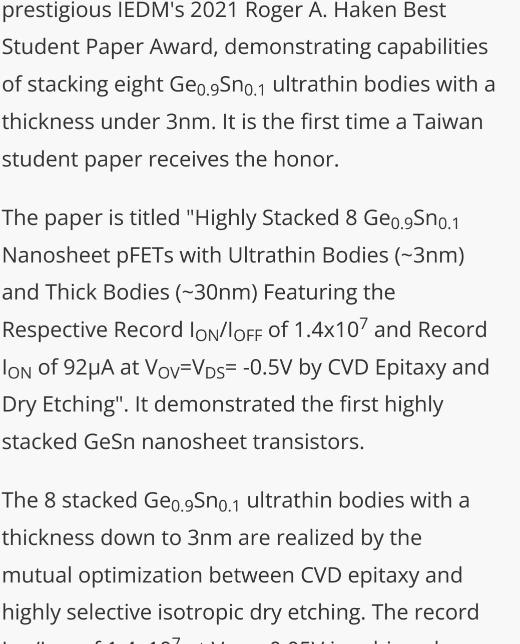
Taiwan's award-winning student paper shows breakthrough in stacking GeSn nanosheet transistors

Judy Lin, DIGITIMES Asia, Taipei

Tuesday 6 December 2022

0





Credit: Tsai Chung-en

A National Taiwan University (NTU) student research paper won the semiconductor industry's prestigious IEDM's 2021 Roger A. Haken Best Student Paper Award, demonstrating capabilities of stacking eight $Ge_{0.9}Sn_{0.1}$ ultrathin bodies with a thickness under 3nm. It is the first time a Taiwan student paper receives the honor.

The paper is titled "Highly Stacked 8 $Ge_{0.9}Sn_{0.1}$ Nanosheet pFETs with Ultrathin Bodies (~3nm) and Thick Bodies (~30nm) Featuring the Respective Record I_{ON}/I_{OFF} of $1.4x10^7$ and Record I_{ON} of 92μA at V_{OV}=V_{DS}= -0.5V by CVD Epitaxy and Dry Etching". It demonstrated the first highly stacked GeSn nanosheet transistors.

The 8 stacked $Ge_{0.9}Sn_{0.1}$ ultrathin bodies with a thickness down to 3nm are realized by the mutual optimization between CVD epitaxy and highly selective isotropic dry etching. The record I_{ON}/I_{OFF} of $1.4x10^7$ at V_{DS}= -0.05V is achieved among GeSn/Ge 3D pFETs thanks to the reduced I_{OFF} by quantum confinement in the 3nm GeSn ultrathin bodies. The record I_{ON} of 92μA per stack at V_{OV}=V_{DS}= -0.5V is achieved among all GeSn/Ge 3D pFETs for the thick nanosheets. These 8 stacked channels are the tallest among pFETs.

The IEEE IEDM conference committee says that the best papers are chosen based on the scientific impact of the abstract, combined with the quality of the oral presentation of the student at IEDM.

First author Tsai Chung-en, a Ph.D. student trained in the Advanced Silicon Device and Process Laboratory of National Taiwan University, received the award with his colleagues and advisor professor Chee Wee Liu on December 5 at Hilton San Francisco Union Square.

Tsai's paper showed the result of their experiment achieving a world record of driving current (I_{ON}) for a Sn/Germanium three-dimensional P-type transistor by integrating a high number (eight-layer) nanosheet with a high mobility channel of Germanium-Sn, and optimizing the epitaxy and etching process to produce an extremely thin channel with a thickness of 3 nm.

In addition, at VLSI 2022, the same NTU team further demonstrated the world record of eight-layer stacked germanium-tin ultra-thin channel transistors with an average channel thickness of 2.4 nm and a subthreshold swing of 64 mV/dec. The average channel thickness is 2.4nm, and the sub-critical oscillation is nearly ideal at 64mV/dec. It is proven by simulation that the extremely thin channel can improve the injection velocity and reduce the intrinsic gate delay, which is the development trend of short channel components.

In an email interview with DIGITIMES, Tsai said that he was surprised that his paper had won the 2021 IEDM Best Student Paper Award, as previous winners all came from top foreign schools such as MIT and the University of Tokyo. This is the first time that a university in Taiwan has been honored with this award. "We thank Prof. Chee Wee Liu for his guidance and appreciate our lab colleagues for teamwork. Thanks to our family and friends for their support, and everyone who has helped us. We hope that Taiwan will continue to lead the world in semiconductor progress and growth, and contribute to a better life for all people," said Tsai.

Advisor of the team, Chee Wee Liu, who is a distinguished professor and the CEO of the Advanced Silicon Device and Process Laboratory of National Taiwan University, takes pride in his students and said he encourages students with his motto: "Never give up your dream!" Liu told DIGITIMES his basic requirement for students in his lab is integrity, accountability, teamwork, and a love for research.

The International Electron Devices Meeting (IEDM), sponsored by the Institute of Electrical and Electronic Engineers (IEEE)'s Electronic Devices Society (EDS) and held annually in December in the United States, is the world's leading scientific and technical forum for technological breakthroughs in semiconductor and electronic device technology, design, fabrication, physics, and modeling. IEDM is a leading international conference that brings together the best engineers and scientists from industry and academia around the world. This year's 68th IEDM is be held December 3-7, 2022, at the Hilton San Francisco Union Square, with the theme "the 75th Anniversary of the Transistor, and the Next Transformative Devices to Address Global Challenges".

With the evolution of semiconductor process technology nodes, the transistor structure in the chip from the traditional Planar FET to the mainstream FinFET, to the future TSMC 2 nanometer technology node will use the gate-all-around (GAA) stacked nanosheet transistors (stacked Nanosheet transistors are designed for higher logic density, faster speed, and lower power consumption to provide high-performance computing and mobile communication applications such as 5G, electric vehicles, AI, and the metaverse). In order to improve the logic density, the size of transistors continues to shrink. However, the problem of a larger leakage current will arise. The gate oxide layer and the gate metal completely cover all the channels of the gate-all-around transistors, making the channels more controllable, effectively reducing leakage current and power consumption, and making the transistors more energy efficient and power saving. For higher performance and faster operation, channel stacking technology (stacking more channels vertically) and high mobility channels such as silicon germanium (SiGe), germanium (Ge), and germanium tin (GeSn) can be used to increase the driving current of the transistors.

Due to the quantum limit effect, the leakage current of the transistor is greatly reduced, and the switching current ratio (I_{ON}/I_{OFF}) is improved to a world record of > 107. This IEDM paper provided a complete discussion and analysis of epitaxial layer design and growth, material analysis, etching mechanism, electrical analysis, band gap simulation, strain simulation, and variable temperature measurement, etc. This paper integrates the characteristics of high number, high mobility channels, and extremely thin channels to demonstrate the world's first high number stacked germanium-tin nanosheet transistors, which can enhance the driving current and reduce the leakage current, resulting in higher performance of semiconductor wafers and more energy saving. It will also be more energy efficient.

Currently, NTU is one of the few universities (outside the industry) that can independently develop multi-layer stacked channel gate-all-around transistors. "In the future, we will be able to bring our experience and knowledge to solve real problems," said Tsai, who is now working at TSMC as a research engineer.

Categories Chips + components | IC design, distribution | IC manufacturing | Passive, PCB, other IC components

Tags DeepTech | Taiwan

Share this article

Other links

Print

Related content